REMARKS

This paper is submitted in reply to the Office Action dated September 6, 2005, within the three-month period for response. Reconsideration and allowance of all pending claims are respectfully requested.

In the subject Office Action, claims 19-21 were rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Moreover, claims 1-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,404,563 to Green et al. (Green) in view of U.S. Patent No. 5,872,963 to Bitar et al. (Bitar).

Applicants respectfully traverse the Examiner's rejections to the extent that they are maintained. Applicants have nonetheless amended claims 1, 11 and 19 in deference to, and in some cases, as suggested by the Examiner. Claim 20 has been canceled to further put the case in condition for allowance. Applicants respectfully submit that no new matter is being added by the above amendments, as the amendments are fully supported in the specification, drawings and claims as originally filed.

Now turning to the art-based rejections in the subject Office Action, and more specifically to the rejection of independent claim 1, this claim generally recites a method for yielding a virtual processor within a logically partitioned data processing system, wherein the system supports a plurality of partitions, a first of which includes a plurality of virtual processors that share at least one CPU. As amended, the virtual processors comprise entities used to schedule threads. The method further includes requesting with a yielding virtual processor a yield of the CPU upon which the virtual processor is executing, including designating a target virtual processor from among the plurality of virtual processors. The method also includes switching-in the target virtual processor for execution by the CPU in response to the requested yield.

The amended claim language recites the function of a virtual processor for use in scheduling thread execution. Conventional operating systems dispatch threads (units of execution) to CPU's. In a logically partitioned system, the operating system thinks that

virtual processors are CPU's for purposes of dispatching threads. That is, the operating system dispatches threads to virtual processors. The hypervisor schedules CPU resources to the virtual processors to execute the threads dispatched to the virtual processors. As such, the virtual processor is used (by the hypervisor) to schedule thread execution.

None of the cited prior art discloses the claimed feature of scheduling virtual processors (that, in turn, are used to schedule threads). For instance, the disclosure of Bitar et al. is limited to scheduling threads, not virtual processors. As outlined in Bitar et al., a virtual processor is not the same as a (user) thread (column 1, lines 32-33). Fig. 2b of Bitar et al. further illustrates this distinction in showing threads 2 mapped to kernel space comprising virtual processors 5 (column 5, lines 64-65). Fig. 8 likewise shows threads 24.M switched without using kernel space 18 (and associated virtual processors 45). As claimed, a virtual processor is used to schedule threads (a scheduling entity), and it not an executing entity (as Bitar et al. defines threads at column 1, lines 17-19). Notably, Bitar et al. seeks to have threads executed by the CPU without using the virtual processor (or other scheduling entities, i.e., kernel thread) for efficiency considerations (column 5, lines 31-33 and lines 55-58).

Perhaps some confusion has arisen due to the disclosure in Bitar et al. that describes a kernel thread in a Mach operating system as being the equivalent of a virtual processor in other operating systems (column 1, lines 54-column 2, line 5). However, Bitar et al. characterizes both the kernel thread and the virtual processor as being "the basic unit of scheduling." What these units are being used to schedule, or map, are user threads. As the claims now explicitly recite the function of the virtual processor as a entity used for scheduling, Applicants respectfully submit that the functional distinction between a virtual processor and a thread is patentably clear.

While Green et al. introduces the general concept of hypervisors, the Examiner notes that Green does not disclose the claimed use of virtual processors to schedule threads. As such, any combination of Bitar et al. with Green et al. will still fail to suggest

or motivate switching-in a virtual processor used to schedule a thread. Reconsideration and allowance of claim 1, as well as of claims 2-10 that depend therefrom, are therefore respectfully requested.

Independent claim 11 is a computer hardware and software implementation configured to execute method steps similar to those recited in claim 1. Claim 11 is therefore similarly non-obvious over the cited prior art for reasons similar to those discussed in the context of claim 1, and reconsideration and allowance of claim 11, as well as of claims 12-18 and 21 that depend therefrom, are respectfully requested.

Independent claim 19 is basically a program product implementation configured to execute method steps similar to those recited in claim 1. Claim 19 is therefore similarly non-obvious over the cited prior art, and the reconsideration and allowance of claim 19 are respectfully requested.

As a final matter, Applicants respectfully request the Examiner consider the references cited in the Information Disclosure Statements filed by Applicants on March 7, 2005, May 18, 2005, June 8, 2005 and September 19, 2005, all of which are available on PAIR, and return initialed copies to Applicants in the Examiner's next communication.

In summary, Applicants respectfully submit that all pending claims are novel and non-obvious over the prior art of record. Reconsideration and allowance of all pending claims are therefore respectfully requested. If the Examiner has any questions regarding the foregoing, or which might otherwise further this case onto allowance, the Examiner may contact the undersigned at (513) 241-2324. Moreover, if any other charges or credits

are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,

12/6/05
Date

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